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Proposal for unified system design meta flow in task-level instruction-level design technology research for multi-media applications

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Abstract

This paper describes an attempt to bring together the many different system design flows architecture and system design technology research, into a more abstract but unifying meta flow. Since system and architecture design flows have a strong resemblance and unnecessary overlap, lack of a common and consistent terminology coupled to a common reference basis, it is difficult to compare and reuse (sub)steps. In addition, there is a too strong separation between research communities. To alleviate this problem, we introduce a more abstract but unifying meta flow to bridge the gap between the existing flows. From this meta flow, a particular design flow can be derived for a given application (domain) by leaving out the non-required stages/steps, by selecting a subset which is compatible with the partial meta-flow order, and by selecting the appropriate technology remaining (sub)steps (e.g. the type of scheduler). This paper focuses on the principles at instruction-level abstractions. It also provides an illustration of the power of the meta-flow approach using a realistic multi-media compression demonstrator from the MPEG4 context.

Index Terms

Indexing

Controlled Indexing

[embedded systems](#) [high level synthesis](#)

Non-controlled Indexing

[instruction-level](#) [meta flow](#) [multi-media applications](#) [task-level](#) [unified system](#)

Author Keywords

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References

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Citing Documents

- 1 System-on-chip design: impact on education and research, De Man, H.
Design & Test of Computers, IEEE
On page(s): 11-19, Volume: 3, Issue: 3, 1999
[Abstract](#) | Full Text: [PDF](#) (96)
- 2 Dynamic memory management methodology applied to embedded telecom network systems
Couvreur, C.; Lambrecht, J.; Verkest, D.; Cattoor, F.; Svantesson, B.; Hemani, A.; Van den Broeck, P.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
On page(s): 650- 667, Volume: 10, Issue: 5, Oct 2002
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Task concurrency management experiment for power-efficient speed-up of embedded MPEG4 IM1 player

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Abstract

Addresses the concurrent task management of complex multimedia systems, like the MP (Implementation 1) player. Starting with a critical part of the code in the IM1 player, we expose concurrency hidden by implementation decisions and represented it with our "grey-box" model. Based on this "grey-box" model, high-level transformations have been made to improve task scheduling the transformed graph, we have improved the performance of an important block layer of the IM1 player while simultaneously lowering the system energy cost. A two-processor is used in the experiment, combining processors running at a high V_{dd} (drain supply voltage) respectively

Index Terms

Inspec

Controlled Indexing

[concurrency control](#) [embedded systems](#) [multimedia systems](#) [performance evaluation](#) [video coding](#) [video equipment](#)

Non-controlled Indexing

[complex multimedia systems](#) [concurrent task management](#) [drain supply voltage](#) [MPEG4 IM1 player](#) [grey-box model](#) [high-level transformations](#) [implementation](#) [power-efficient speedup](#) [system energy cost](#) [system layer performance](#) [task management](#) [transformed graph scheduling](#) [two-processor target platform](#)

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References

No references available on IEEE Xplore.

Citing Documents

- 1 Energy-aware runtime scheduling for embedded-multiprocessor SOC's, Peng Yang; Marchal, P.; Catthoor, F.; Desmet, D.; Verkest, D.; Lauwereins, R. *Design & Test of Computers, IEEE* On page(s): 46-58, Volume: 18, Issue: 5, Sep-Oct 2001 [Abstract](#) | Full Text: [PDF](#) (200)

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